Amendments to the Specification

Please replace the paragraph beginning on page 9, line 13, with the following rewritten paragraph:

As shown in FIGS. 3 and 4, in the data "0" write period in the first half of the program cycle, 0 V is applied to the selected bitline connected with the ferroelectric capacitor in which data "0" should be written (selected memory cell), and Vs (power supply voltage Vcc, for example) is applied to the selected wordline. The polarization state is moved from the point B or D to the point A in FIG. 2 by applying +Vs to the selected memory cell, whereby data "0" is written into the selected memory cell. ~~2Vs/3 is~~ 2/3 Vs is applied to the unselected bitlines connected with the unselected memory cells, ~~and Vs/3~~ and 1/3 Vs is applied to the unselected wordlines. Therefore, ~~±Vs/3~~ ± 1/3 Vs is applied to the unselected memory cells, whereby the memory state is maintained.

Please replace the paragraph beginning on page 9, line 22 - page 10, line 3, with the following rewritten paragraph:

In the data "1" write period in the latter half of the program cycle, Vs (power supply voltage Vcc, for example) is applied to the selected bitline connected with the ferroelectric capacitor in which data "1" should be written (selected memory cell), and 0 V is applied to the selected wordline. The polarization state is moved from the point B or D to the point C in FIG. 2 by applying -Vs to the selected memory cell in this manner, whereby data "1" is written into the selected memory cell. ~~Vs/3 is~~ 1/3 Vs is applied to the unselected bitlines connected with the unselected memory cells, and ~~2Vs/3 is~~ 2/3 Vs is applied to the unselected wordlines. Therefore, ~~±Vs/3 is~~ ± 1/3 Vs is applied to the unselected memory cells, whereby the memory state is maintained.

Please replace the paragraph beginning on page 11, line 25, with the following rewritten paragraph:

A power supply circuit 180 shown in FIG. 7 generates various voltages described with reference to FIGS. 3 to 6 ~~(Vs, 2Vs/3,Vs/3,~~ (Vs, 2/3 Vs, 1/3 Vs, and 0, for example), and supplies the voltages to the X and Y decoders 100 and 110.

Please replace the paragraph beginning on page 15, line 6, with the following rewritten paragraph:

If the judgment in the step 11 in FIG. 15 is NO, the step 10 cannot be performed since the program data (PD) does not exist. Therefore, the operation waits for input of the program data (PD). All of the memory cells are set in the standby state (S) in the step 12 in FIG. 15 during the wait period. In the standby state (S), the voltage applied to all of the memory cells is set at 0 V. Therefore, since a disturbance voltage is not applied to the ferroelectric capacitors 50, a decrease in data read margin or destruction of data does not occur. If the memory cells are not set in the standby state, the unselected voltage ~~Vs/3 is~~ 1/3 Vs is continuously applied to the unselected memory cells, whereby the polarization of the ferroelectric capacitors 50 deteriorates and the data read margin decreases. In the worst case, data is destroyed (data "0" and "1" cannot be distinguished).